forming an insulation layer outwardly from the substrate, the insulation layer filling the isolation trenches and covering the active areas and substantially conforming to the substrate surface contour;

forming a planarization layer outwardly from the insulation layer, the planarization layer having an outward surface that is substantially flat; and

removing the planarization layer and the insulation layer by a removing process that removes the planarization layer and the insulation layer at substantially the same rate.

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2. The method of Claim 1, wherein removing the planarization layer and the insulation layer further comprises:

etching through the planarization layer and the insulation layer together down to a chemical mechanical polishing (CMP) depth outward from the active areas; and

chemically-mechanically polishing from the CMP depth down to the polish stop layer above the active areas.

anti precedent

13. A method for forming an integrated circuit, comprising:

forming a plurality of isolation trenches in a substrate, the isolation trenches separating active areas;

forming an insulation layer outwardly from the substrate, the insulation layer filling the isolation trenches and covering the active areas and substantially conforming to the substrate surface contour;

forming a planarization layer outwardly from the insulation layer, the planarization layer having an outward surface that is substantially flat;

etching through the planarization layer and the insulation layer by an etching process that etches the planarization layer and the insulation layer at substantially the same rate, down to a chemical mechanical polishing (CMP) depth outward from the active areas;

chemically-mechanically polishing from the CMP depth down to a polish stop for the active areas; and

forming integrated circuit devices in the active areas to form an integrated circuit on the substrate.

14. The method of Claim 13, further comprising etching through the planarization layer and the insulation layer using a matched etch process that etches the planarization layer and the insulation layer at rates that differ by ten percent or less.

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15. The method of Claim 13, further comprising etching through the planarization layer and the insulation layer using a matched etch process that etches the planarization layer and the insulation layer at rates that differ by five percent or less.